



### Overview:

The VXL Direct Digital Synthesizer (DDS) is an IP core for digitally creating arbitrary waveforms and frequencies from a single, fixed source frequency. This DDS system takes a constant reference clock input and scales it down to a specified output frequency sampled at the reference clock frequency. This method of frequency control makes the IP core ideal for systems that require precise frequency sweeps like Radars.

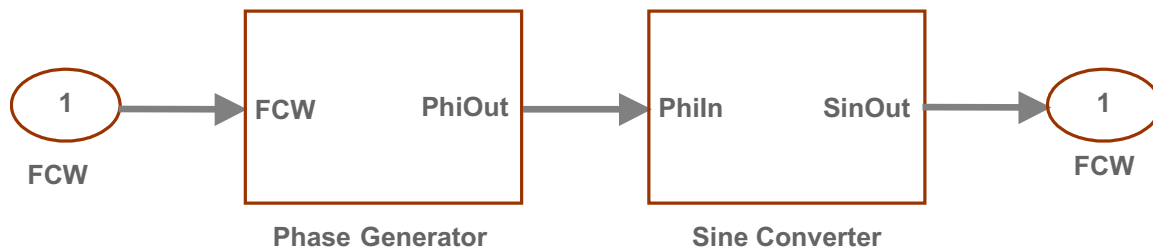
### Features:

- Implemented using Piecewise Quadrature Sine Interpolation (PQSI) algorithm
- Sixteen segments per quadrature
- 1024 points per segment
- Very low memory requirements of 704 bits
- User selectable output resolution of 12 to 20 bits.
- Pipeline delay of 16/17 clocks for signed/unsigned output
- FCW (Frequency Control Word) resolution of 16 to 32 bits
- Low SFDR (Spurious Free Dynamic Range), better than 96 dBc for output frequency range of 0.15 fclk to 0.20 fclk

### Key Benefits:

- Low memory requirements
- High speed capabilities
- Technology independent IP core
- Highly optimized design with minimum usage of target device resources
- Parameterized HDL design
- Easily modifiable to meet specific client requirements
- RTL source code available for easy integration and implementation

### Block diagram:

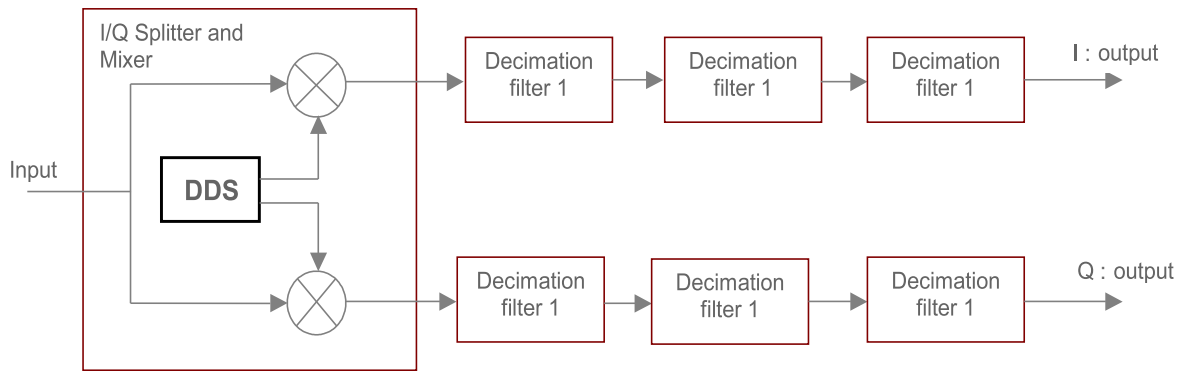


### Applications:

- Digital radios and modems
- Software-Defined Radio's (SDR)
- Digital up/down converters for cellular and PCS base stations
- Waveform synthesis in Digital Phase Locked Loops
- Generating injection frequencies for analog mixers

### Application Note - Digital Down Converter (DDC):

DDC is composed of an I/Q splitter incorporating a DDS. DDC modulates the input signal coming from the RF section with sine and cosine waves by utilizing two mixers and a decimation section consisting of a series of FIR decimation filters.



**Deliverables:**

- Core options
  - RTL design in VHDL
  - Technology specific netlist
- Test bench
- Documentation

**Target Technologies:**

- **FPGA:** Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

**Device utilization summary:**

Target Device	Max. Frequency (MHz)	Slices used	18x18 Multipliers
Xilinx Spartan XC3S400	165	334	3

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