

**Overview:**

The VXL Generic Framing Protocol (GFP) IP core implements the ITU-T G.7041 communication standard. The GFP IP core operates in PDU oriented adaptation mode, referred to as Frame Mapped GFP (GFP – F) mode. The IP core consists of a transmission and a reception unit that enable the transmission and reception of data to or from a SONET/SDH network. The GFP-F Encapsulation core receives data from the client network over an Ethernet interface, encapsulates the data according to GFP protocol, and transmits the GFP encapsulated data frame. The GFP-F Decapsulation core receives the GFP encapsulated data frames from higher network layer, de-maps the GFP frames to extract client network data to be transmitted over an Ethernet interface.

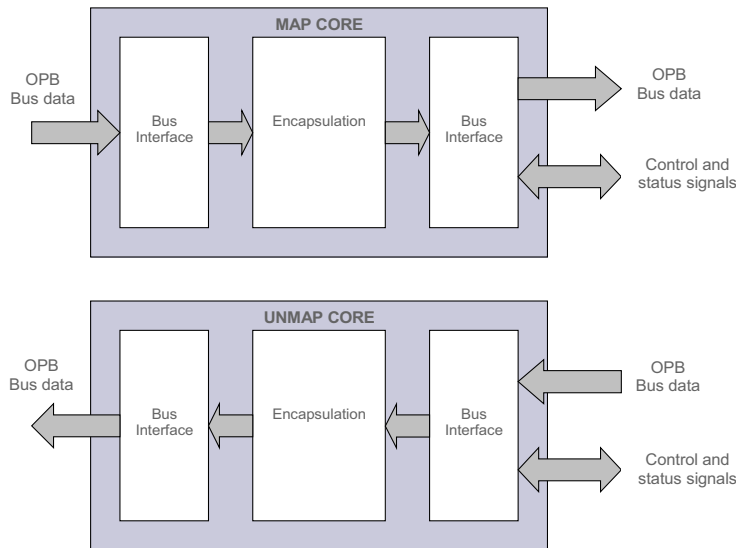
**Features:**

- Implements the ITU–T G.7041 GFP Specification
- Frame mapped GFP (GFP – F) support
- Ethernet with null frames support
- Client data frames support
- Local Link Interfaces for data transfer
- Single bit error correction for Type Header and Core Header using CRC 16

**Key Benefits:**

- Customizable HDL design
- High data rate capabilities
- Supports all frame mapped protocols defined in the ITU-T GFP specification including PPP, Ethernet and RPR.
- RTL source code available for easy integration and implementation.

**Block diagram:**

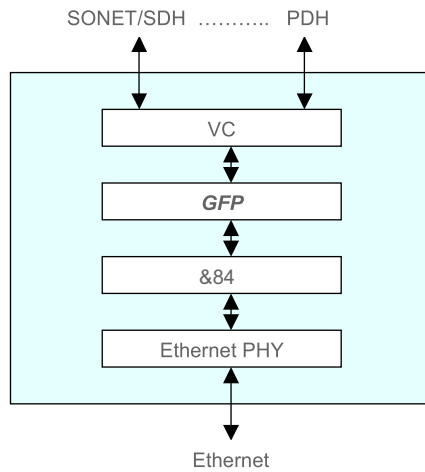


**Applications:**

- Transport of IP/Ethernet Protocols over SONET/SDH/PDH
- Transport of LAN/SAN over SONET/SDH/PDH

**Application Note – Ethernet to PDH mapper:**

Ethernet–PDH mapper provides GFP–F mapping of Ethernet traffic into PDH signals. Ethernet– PDH is a protocol converter that transports Ethernet services over existing PDH signal formats.



**Deliverables:**

- Core options
  - RTL design in VHDL
  - Technology specific netlist
- Test bench
- Documentation

**Target Technologies:**

- **FPGA:** Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

**Device utilization summary:**

*Encapsulation Side:*

Target Device	Max. Frequency (MHz)	Slices used	Block RAMs
Xilinx Spartan 3S1500FG456-5	86	805	3

*Decapsulation Side:*

Target Device	Max. Frequency (MHz)	Slices used	Block RAMs
Xilinx Spartan 3S1500FG456-5	78	553	-

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