JPEG 2000 Encoder

IP Core *Product Brief*

Overview:

The VXL JPEG 2000 IP core is a JPEG 2000-ISO/IEC 15444-1 compliant encoder. The JPEG 2000 operates on a single clock domain and it can be easily integrated into any multimedia system. A synchronous Reset signal is also provided. The core is efficiently designed, synthesized for Xilinx FPGA target technology and thoroughly verified. The JPEG 2000 IP core is available in VHDL RTL source code.

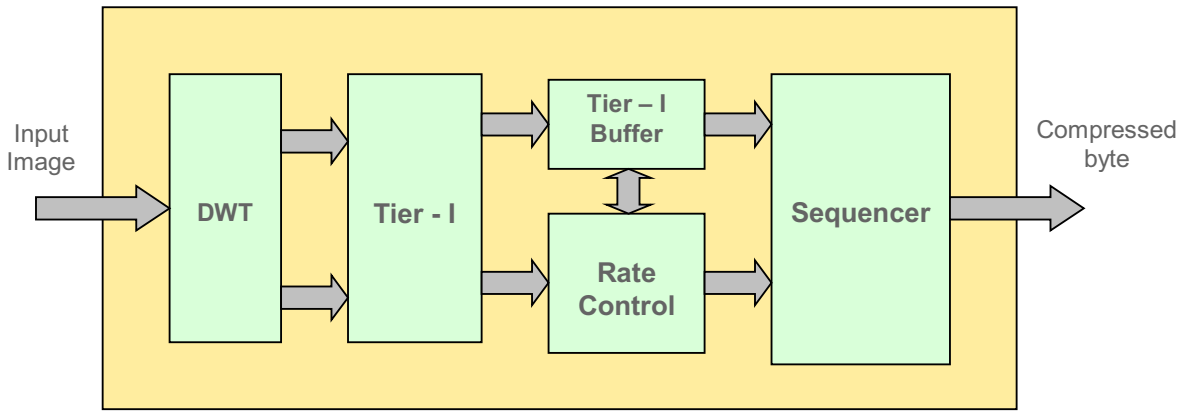
Features:

- JPEG2000-ISO/IEC 15444-1 standard compliant
- User selectable lossless and lossy compression
- Rate Control
- Programmable bit rate up to 10 bits per sample
- Programmable image/tile size up to 8192 x 512
- JPEG2000 graphics file format (.j2k) output
- Large Frames Processing without unpleasant Blocking Artifacts
- Fairly brisk input pixel rate in excess of 100 MSamples/Sec
- Fully synchronous single clock design.
- Internal Memory System architecture

Key Benefits:

- Low target device memory and logic silicon footprint
- Motion JPEG support available (optional)
- Bit equivalent C model provided
- Parameterizable HDL design,
- Easily modifiable design to meet specific requirements
- Available for Xilinx Virtex-4 & 5 series FPGA devices
- RTL source code available for easy integration and implementation

Block diagram:



Applications:

- Consumer Electronics (Digital Cameras, Mobile Phones, Printers, Scanners)
- Client/Server communication (Internet, Image database, Video Streaming)
- Military, Digital CCTV and surveillance systems (HD Satellite Images, Motion detection)
- Medical Imagery
- Remote Sensing
- High Quality Frame based Image/Video recording, editing and storage systems.

Application Case Study – Digital Image Distribution:

This application implements an intelligent image transport system for the Video Surveillance, Defence, Space and Telecom industry. It involves compression of the input image stream using the JPEG 2000 IP core and transmission of the compressed image over Ethernet or a digitally modulated wireless protocol.

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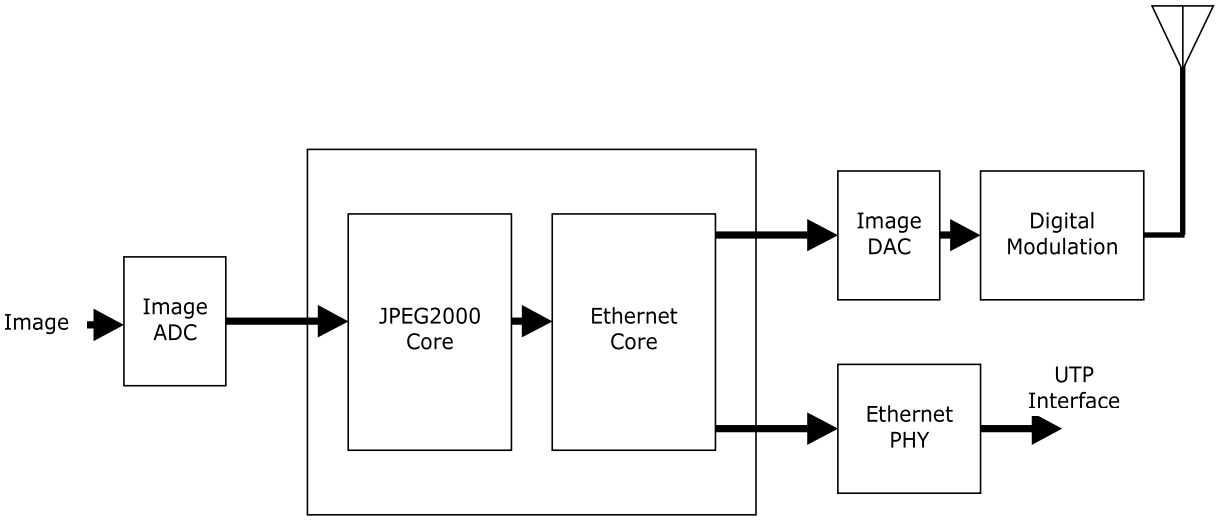

Deliverables:

- Core options
  - RTL design in VHDL
  - Technology specific netlist
- Bit equivalent C model
- Test bench
- Documentation

Target Technologies:

- **FPGA:** Virtex 4, Virtex 5
- ASIC standard cell

Device utilization summary: ***

Target Device	Max. Frequency (MHz)	Slices used	Block RAMs
Xilinx Virtex xc5vlx330t-2-ff1738	105	90845	262

*** 10 bits per pixel; 5/3 DWT type

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